EEDG/CE 6303: Testing and Testable Design (Spring’2023) Department of Electrical & Computer Engineering

The University of Texas at Dallas

**Instructor: Mehrdad Nourani (nourani@utdallas.edu)**

**Cover Page for All Submissions**

**(Assignment, Project, Codes/Simulations/CAD, Examinations, etc.)**

**Last Name (as shown in the official UT Dallas Student ID Card): ANNADATA**

**First Name: YAGNA SRINIVASA HARSHA**

**Submission Materials for (e.g. Homework #, Project #): Homework#3**

**Statement of Academic Honesty**

I certify that:

1. the attached report (for assignment, project, codes/simulations/CAD, examinations, etc.) is my own work, based on my personal study and/or research,
2. I have acknowledged all material and sources used in its preparation, whether they be books, articles, reports, lecture notes, and any other kind of document, electronic or personal communication,
3. this report has not previously been submitted for assessment in EEDG/CE 6303 or any other course at UT Dallas or elsewhere,
4. I have not copied in part or whole or otherwise plagiarized the work of other students and/or persons, and
5. I have read and understood the Department and University policies on scholastic dishonesty as outlined in: [http://www.utdallas.edu/deanofstudents/dishonesty/.](http://www.utdallas.edu/deanofstudents/dishonesty/)

Name: Yagna S H Annadata Date:03/23/2023

Signature:

Q3:

Verilog code:

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 03/23/2023 07:28:08 PM

// Design Name:

// Module Name: Assignment3\_q3

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module Assignment3\_q3(

input x1,

input x2,

input x3,

input clk,

output wire z );

wire c1,c2,c3,Y1,y1;

GTECH\_NOR2 (x1,x2,c1);

assign c2 = c1;

assign c3 = c1;

GTECH\_NOR2 (c3,x3,Y1);

GTECH\_FD1 (Y1,clk,y1);

GTECH\_OR2 (y1,c2,z);

Endmodule

Tetramax Report:

TetraMAX(R)

Version O-2018.06-SP1 for linux64 - Jul 19, 2018

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or distribution of this software is strictly prohibited.

Tcl mode is on by default. Use -notcl to run in native mode.

Executing startup file "/proj/cad/synopsys/synopsys\_2018/tmax\_vO-2018.06-SP1/admin/setup/tmaxtcl.rc".

BUILD-T> set\_faults -report collapsed -fault\_coverage

Warning: Unused gate deletion affects fault coverage calculation. (M245)

BUILD-T> read\_netlist /home/011/y/yx/yxa210024/spring23/testing/LIB/class.v

Begin reading netlist ( /home/011/y/yx/yxa210024/spring23/testing/LIB/class.v )...

End parsing Verilog file /home/011/y/yx/yxa210024/spring23/testing/LIB/class.v with 0 errors.

End reading netlist: #modules=129, top=BIDI, #lines=1039, CPU\_time=0.00 sec, Memory=0MB

BUILD-T> read\_netlist /home/011/y/yx/yxa210024/spring23/testing/src\_ver/gtech\_lib.v

Begin reading netlist ( /home/011/y/yx/yxa210024/spring23/testing/src\_ver/gtech\_lib.v )...

Warning: Rule N2 (unsupported construct) was violated 10 times.

End parsing Verilog file /home/011/y/yx/yxa210024/spring23/testing/src\_ver/gtech\_lib.v with 0 errors.

End reading netlist: #modules=106, top=GTECH\_ZERO, #lines=1976, CPU\_time=0.01 sec, Memory=0MB

BUILD-T> read\_netlist /home/011/y/yx/yxa210024/Assignment3\_q3\_1.v

Begin reading netlist ( /home/011/y/yx/yxa210024/Assignment3\_q3\_1.v )...

End parsing Verilog file /home/011/y/yx/yxa210024/Assignment3\_q3\_1.v with 0 errors.

End reading netlist: #modules=1, top=Assignment3\_q3\_1, #lines=19, CPU\_time=0.00 sec, Memory=0MB

BUILD-T> run\_build\_model Assignment3\_q3\_1

------------------------------------------------------------------------------

Begin build model for topcut = Assignment3\_q3\_1 ...

------------------------------------------------------------------------------

There were 3 primitives and 0 faultable pins removed during model optimizations

Warning: Rule N20 (underspecified UDP) was violated 1 times.

End build model: #primitives=14, CPU\_time=0.00 sec, Memory=0MB

------------------------------------------------------------------------------

Begin learning analyses...

End learning analyses, total learning CPU time=0.00 sec.

------------------------------------------------------------------------------

DRC-T> set\_drc /home/011/y/yx/yxa210024/Assignment3\_q3\_1.stil

DRC-T> run\_drc

------------------------------------------------------------------------------

Begin scan design rules checking...

------------------------------------------------------------------------------

Begin reading test protocol file /home/011/y/yx/yxa210024/Assignment3\_q3\_1.stil...

End parsing STIL file /home/011/y/yx/yxa210024/Assignment3\_q3\_1.stil with 0 errors.

Test protocol file reading completed, CPU time=0.00 sec.

------------------------------------------------------------------------------

Begin simulating test protocol procedures...

Test protocol simulation completed, CPU time=0.00 sec.

------------------------------------------------------------------------------

Begin scan chain operation checking...

Chain 1 successfully traced with 1 scan\_cells.

Scan chain operation checking completed, CPU time=0.00 sec.

------------------------------------------------------------------------------

Begin clock rules checking...

Clock rules checking completed, CPU time=0.00 sec.

Clock grouping results: #pairs=0, #groups=0, #serial\_pairs=0, #disturbed\_pairs=0, CPU time=0.00 sec.

------------------------------------------------------------------------------

Begin nonscan rules checking...

Nonscan cell summary: #DFF=0 #DLAT=0 #RAM\_outs=0 tla\_usage\_type=none

Nonscan rules checking completed, CPU time=0.00 sec.

------------------------------------------------------------------------------

Begin DRC dependent learning...

Fast-sequential depth results: control=0(0), observe=0(0), detect=0(0), CPU time=0.00 sec

DRC dependent learning completed, CPU time=0.00 sec.

------------------------------------------------------------------------------

DRC Summary Report

------------------------------------------------------------------------------

No violations occurred during DRC process.

Design rules checking was successful, total CPU time=0.00 sec.

------------------------------------------------------------------------------

TEST-T> remove\_faults -all

0 faults were removed from the fault list.

TEST-T> add\_faults -all

22 faults were added to fault list.

TEST-T> run\_atpg -ndetects 1

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\* NOTICE: The following DRC violations were previously \*

\* encountered. The presence of these violations is an \*

\* indicator that it is possible that the ATPG patterns \*

\* created during this process may fail in simulation. \*

\* \*

\* Rules: N20 \*

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

ATPG performed for stuck fault model using internal pattern source.

----------------------------------------------------------

#patterns #faults #ATPG faults test process

stored detect/active red/au/abort coverage CPU time

--------- ------------- ------------ -------- --------

Begin deterministic ATPG: #collapsed\_faults=13, abort\_limit=10...

7 13 0 0/0/0 100.00% 0.00

Collapsed Stuck Fault Summary Report

-----------------------------------------------

fault class code #faults

------------------------------ ---- ---------

Detected DT 22

Possibly detected PT 0

Undetectable UD 0

ATPG untestable AU 0

Not detected ND 0

-----------------------------------------------

total faults 22

test coverage 100.00%

fault coverage 100.00%

-----------------------------------------------

Pattern Summary Report

-----------------------------------------------

#internal patterns 7

#basic\_scan patterns 7

-----------------------------------------------

TEST-T>

Schematic:

Diagram

Description automatically generated with low confidence

Q6:

Verilog code:

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 03/23/2023 05:36:47 PM

// Design Name:

// Module Name: Assignment3\_6que

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module Assignment3\_6que(

input x1,

input x2,

input x3,

output wire z );

wire c1,c2,c3,c4,c5;

GTECH\_NAND2 (x1,x1,c1);

GTECH\_AND2 (c1,x2,c2);

GTECH\_OR2 (c2,x3,c3);

GTECH\_AND2 (c3,x2,c4);

GTECH\_OR2 (c3,x3,c5);

GTECH\_NAND2 (c4,c5,z);

Endmodule

Synopsys code:

/////////////////////////////////////////////////////////////

// Created by: Synopsys DC Expert(TM) in wire load mode

// Version : O-2018.06-SP1

// Date : Thu Mar 23 18:00:23 2023

/////////////////////////////////////////////////////////////

module Assignment3\_6que\_1 ( x1, x2, x3, z );

input x1, x2, x3;

output z;

wire n2;

GTECH\_NAND2 U3 ( .A(n2), .B(x2), .Z(z) );

GTECH\_OR\_NOT U4 ( .A(x3), .B(x1), .Z(n2) );

Endmodule

Pathfile:

$path {

$name path1rising;

$transition{

x1 ^;

tmp101/U1/Z v;

tmp102/U1/Z v;

tmp103/U1/Z v;

tmp104/U1/Z v;

tmp105/U1/Z ^;

tmp105 ^;

$condition{

x2 11;

x3 00;

}

}

$path {

$name path1falling;

$transition{

x1 v;

tmp101/U1/Z ^;

tmp102/U1/Z ^;

tmp103/U1/Z ^;

tmp104/U1/Z ^;

tmp105/U1/Z v;

tmp105 v;

$condition{

x2 11;

x3 00;

}

}

Schematic:

Diagram

Description automatically generated